IN THE SPECIFICATION

Please amend the Title on page 1, line 1, as follows:

NAND TYPE NON-VOLATILE SEMICONDUCTOR MEMORY DEVICE

Please amend the paragraph on page 14, lines 8-24, as follows:

Before data writing, old data stored in the NAND cell block is erased collectively. Thus, all the memory transistors of the block are placed in an all-"1" state where the thresholds are low (for example, negative). Then, "0" or "1" write data is given from the sense amplifier/data latch 2 to the bit lines BL and written sequentially into the respective pages of memory transistors, starting with the page nearest to the common source line SL. ~~FIG. 3 also shows that a control gate line CG1 is selected.~~ At this time, before application of the write voltage, Vss = 0 V and a boosted voltage Vpre higher than Vdd are given to the bit lines BL0 and BL1, respectively. At this time, by applying Vdd + α and Vss to the bit-line side select gate line SGD and the select gate line SGS adjacent to the common source line SL, respectively, the channels of the two NAND cells on the sides of bit lines BL0 and BL1 are precharged to low and high levels, respectively.

Please amend the paragraph on page 14, lines 25-32, as follows:

Thus, the channel of the NAND cell on the side of the bit line BL0 to which the "0" data has been applied is set to a low level Vss whereas the channel of the NAND cell on the side of the bit line BL1 to which the "1" data has been applied is precharged to Vdd or higher. After that, the voltage of the bit line side select gate line SGD is changed from Vdd+α to Vdd. Thus, the select gate transistor SG11 is turned off on the bit line BL1 side, so that the channel of the NAND is placed in the floating state of high level.

Please amend the paragraph on page 15, lines 6-17, as follows:

[[Th]] The reason why the medium voltage Vpass is applied to the control gate lines CG3, CG4, ... , and CG15 is to apply the voltage of the control gate to the substrate through capacitive coupling to thereby surely cut off the channel of a non-selected memory transistor MC 21 adjacent to the selected memory transistor MC11 in the NAND cell connected to the bit line BL to which "1" data is applied. Thus, application of the medium voltage Vpass to all these control gate lines is not necessarily required. The medium voltage may be instead applied to at least one of those control gate lines and Vss may be applied to the remaining control gate lines.